REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-22 are pending in the application. The Examiner additionally stated that claims 1-4, 7, 9, 10, 12, 13, and 18-20 are rejected and claims 5, 6, 8, 11, 14-17, 21, and 22 are objected to. By this amendment, claims 5, 11, and 22 are cancelled and claims 1, 9, and 18 are amended. Hence, claims 1-4, 6-10, and 12-21 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Allowable Subject Matter

The Examiner objected to claims 5-6, 8, 11, 14-17, and 21-22 as being dependent upon a rejected base claim, but indicated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant appreciates the Examiner's consideration and indications of allowability of these claims. By this amendment, the allowable limitations of claim 5 have been incorporated into the language of claim 1, the allowable limitations of claim 11 have been incorporated into the language of claim 9, and the allowable limitations of claim 22 have been incorporated into the language of claim 18. Claims 5, 11, and 22 have been cancelled and those claims depending from claims 5, 11, and 22 have been amended to now depend from claims 1, 9, and 18, as appropriate.

Rejections Under 35 U.S.C. §102(b)

The Examiner rejected claims 1-4, 7, 9-10, 12-13 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Partovi H. et al. ("Flow-through latch and edge-triggered

flip-flop hybrid elements", SOLID-STATE CIRCUITS CONFERENCE, 1996), hereinafter, "Partovi." Applicant respectfully traverses.

Regarding claim 1, the Examiner stated that Fig. 8 of Partovi H. et al. teaches a dynamic logic return-to-zero (RTZ) latching mechanism, comprising: a complementary pair of evaluation devices (first PMOS whose gate coupled to CLK and NMOS whose gate coupled to a three series connected inverter) responsive to a clock signal (CLK); a dynamic evaluator (NMOS coupled to D), coupled between the complementary pair of evaluation devices at a pre-charged node (node coupled to the first PMOS), that evaluates a logic function (buffer) based on at least one input data signal (D); delayed inversion logic (three inverter connected in series provides delay) that receives the clock signal and that outputs an evaluation complete signal being a delayed and inverted version of the clock signal (the output of three series connected inverters) ; and latching logic (full latch comprising two inverters coupled to *Q),* responsive to the evaluation complete signal and the state of the pre-charged node, that asserts the logic state of an output node based on the state of the pre-charged node during an evaluation period between an operative edge of the clock signal and the next edge of the evaluation complete signal, and that returns the output node to zero between evaluation periods (samples the data on the rising edge of the clock and being reset through PRI after a predetermined delay period where the output Q is returns to zero when reset by PRI; last paragraph on page 138).

In reply, Applicant notes that by this amendment, the allowable limitations of claim 5 are incorporated into independent claim 1, thereby rendering claim 1 allowable over the prior art of record. Accordingly, Applicant requests that the rejection of claim 1 be withdrawn.

With respect to claims 2-4 and 7, these claims depend from claim 1 and add further limitations that are neither anticipated nor made obvious by Partovi. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections of claims 2-4 and 7.

Regarding claim 9, the Examiner pointed out that Fig. 8 of Partovi H. et al. teaches a dynamic latch circuit, comprising: a dynamic circuit that pre-charges at least one pre-charged node while a clock signal is low (when CLK is low, first PMOS is turned on and

precharge the node) and that evaluates a logic function for controlling the state of the at least one precharged node when the clock signal goes high (when CLK is high, the precharging is disabled by turning off the first PMOS, and evaluates the input signal D); a delayed inverter receiving the clock signal and providing an inverted delayed clock signal (three inverters coupled in series provides inverted delayed clock); and a latching circuit (two inverters coupled back to back is a full latch with reset PMOS transistor), coupled to the dynamic circuit and the delayed inverter, that controls the state of an output node based on the state of the at least one pre-charged node during each evaluation period beginning when the clock signal goes high and ending when the inverted delayed clock signal next goes low, and that otherwise asserts the output node to a zero logic state (samples the data on the rising edge of the clock and being reset through PRI after a predetermined delay period where the output Q is returns to zero when reset by PRI ; last paragraph on page 138).

In reply, Applicant notes that by this communication, the allowable limitations of claim 11 are incorporated into independent claim 9, thereby rendering claim 9 allowable over the prior art of record. Therefore, Applicant requests that the rejection of claim 9 be withdrawn.

With respect to claims 10 and 12-13, these claims depend from claim 9 and add further limitations that are neither anticipated nor made obvious by Partovi. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections of claims 10 and 12-13.

Regarding claim 18, the Examiner stated that Fig. 8 of Partovi H. et al. teaches a dynamic logic RTZ latching method, comprising: pre-setting a first node while a clock signal is in a first logic state (when CLK is low, the first PMOS turns on and precharges the source node to logic high); dynamically evaluating a logic function to control the logic state of the first node when the clock signal transitions to a second logic state (when CLK is high, the precharging is disabled by turning off the first PMOS, and evaluates the input signal D); delaying and inverting the clock signal and providing a delayed inverted clock signal (three inverters coupled in series provides inverted delayed clock); latching a logic state

of an output node based on the logic state of the first node determined during an evaluation period beginning when the clock signal transitions to the second logic state and ending with the next corresponding transition of the delayed inverted clock signal; and returning the logic state of the output node to a low logic state between evaluation periods (samples the data on the rising edge of the clock and being reset through PRI after a predetermined delay period where the output Q is returns to zero when reset by PRI ; last paragraph on page 138).

Applicant responds that by this communication, the allowable limitations of claim 22 are incorporated into independent claim 18, thereby rendering claim 18 allowable over the prior art of record. Consequently, Applicant requests that the rejection of claim 18 be withdrawn.

With respect to claims 19-20, these claims depend from claim 18 and add further limitations that are neither anticipated nor made obvious by Partovi. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejections of claims 19-20.

CONCLUSIONS

In view of the arguments advance above, Applicant respectfully submits that claims 1-4, 6-10, and 12-21 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
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